PowerPC™

Upgrading 66MHz PowerPC 601™ System Designs to the 100MHz PowerPC 601

Application Note AN-PPC-003

Redesign 66MHz PCLK PowerPC 601 systems for use with the 100MHz PowerPC 601 by changing the power supply and clock generation circuits. The upgraded systems offer increased performance and lower power dissipation.

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February 1995

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1 Overview

Various PowerPC 601 system designs have been developed for the 66MHz 601. These systems can be upgraded to use the 100MHz PowerPC 601 (the 601v, where the v refers to low voltage) by redesigning the power supply and clock generation circuits. Due to the extent and nature of the required changes, the physical design of the system board will change.

The PowerPC 601 66MHz processor is built in 0.65um CMOS technology. The 601v processor (an exact logical duplicate of the 66MHz PowerPC 601) is built in the higher performance IBM Microelectronics 0.5um CMOS technology. The processors share the same functions, signal I/O, and packages. The typical power dissipation of the 601v at 100MHz is half that of the typical 601 operating at 80Mhz. Other differences between the two processors are the power supply voltages, the power supply pinout, the clock frequencies, and the 2X_PCLK receiver. Some setup and hold times are slightly different. See the PowerPC *601 RISC Microprocessor Hardware Specifications* (IBM document MPR601HSU–03) for details. Some of the following design details refer to the design found in the *PowerPC 601 System Design Kit* (IBM document MPRKITV1–01).

The 601v requires two power supply voltages. The upgraded system design supplies V_{DD} (Vdd_{INT}) = 2.5V for the 601v internal circuits and V_{CC} ($Vdd_{I/O}$) = 5.0V for the 601v I/O circuits.

The clock generation circuit has been changed to supply 2X_PCLK = 200MHz, PCLK_EN# = 100MHz, and BLCK_EN# = 50MHz.

2 Power Supply

In the following discussion the terms V_{CC} and V_{DD} are used in place of $Vdd_{I/O}$ and Vdd_{INT} respectively from the *PowerPC 601 RISC Microprocessor Hardware Specifications*.

2.1 Power Supply Requirements

The 3.6V V_{DD} pins of the 601 have been redefined for the 601v, half of them becoming V_{CC} pins ($V_{CC}1$ through $V_{CC}30$) and half becoming the new V_{DD} pins ($V_{DD}1$ through $V_{DD}29$). The upgraded system design requires V_{DD} = 2.5V ±5% for the 601v internal circuits and V_{CC} = 5.0V ±5% for the 601v I/O circuits. The original 3.6V (3.78V maximum) V_{DD} power supply remains in the design to supply power to the IBM27–82650 Bridge and the clock chip. Processor power dissipation in a typical 601v 100MHz system is 3W less than that of a 601 66MHz system.

2.2 Suggested Power Supply Implementation

The upgraded system design still requires the existing 3.6V V_{DD} regulator, and an additional device is required to supply the new 2.5V V_{DD}. The power element of the new regulator can conveniently be mounted on the opposite side of the existing 3.6V regulator power element heat sink, which is sufficient to cool both of the devices. Refer to Figure 1.0 for circuit details.

The power pins of the 601v have been divided into two groups, neither of which connect to the original 3.6V power supply. $V_{DD}1$ through $V_{DD}29$ are wired to the 2.5V power supply. $V_{CC}1$ through $V_{CC}30$ are wired to the 5.0V power supply. The power plane from the power supplies to the 601v should conform to standard low impedance, high frequency design rules, such as were required for the original V_{DD}. Note on Figure 1.0 the power pin assignments of the 601v.

Power supply bypass capacitor placement and value selection also follow the same design rules. Note on Figure 1.0 the recommended number and value of the bypass and recharge capacitors, which should be distributed around the 601v according to standard high frequency design rules.

Pullup resistors attached to the 601v CPU bus can be connected to the 3.6V supply to obtain minimum t_{PHL} times. If the timing of the net is not critical and other considerations warrant it, these resistors can be connected to the 5V supply.

3 Clock Circuits

3.1 Clock Circuit Requirements

The logical clock requirements of the 601v are identical to those of the 601. However, to allow for an expected lower amplitude clock signal at 200MHz and beyond, the 2X_PCLK clock receiver has been redesigned with V_{IL}(max) = 0.6V and V_{IH}(min) = 1.8V.

3.2 Suggested Clock Circuit Implementation

The IBM25JP–CLK01 generates 2X_PCLK frequencies up to 132MHz. For 2X_PCLK operation at 200MHz, Motorola offers the MPC970. In the upgraded system design, the 601v runs at 100MHz, with CPU bus operation at 50MHz. This requires 2X_PCLK = 200MHz, PCLK_EN# = 100MHz, and BCLK_EN# = 50MHz.

The MPC970 also provides PCI clocks, which in the design found in the *PowerPC 601 System Design Kit,* are supplied by an AMCC 4403B–66 PCI clock generator. This chip can be removed from the upgraded system design if the designer wishes to use the PCI clocks supplied by the MPC970. Attention to clock skew issues is important to ensure that the clocks meet the skew requirements of the system.

At the desired frequencies, the MPC970 requires either a 25MHz crystal (in x4 mode) or a 12.5MHz crystal (in x8 mode) to generate the 100MHz PCLK_EN#. Figure 2.0 shows the MPC970 with a 12.5MHz crystal in x8 mode.

Figure 2.0 also shows 54.9Ω series termination resistors connected as close as possible to the MPC970. The value of these resistors is chosen to match the output driver impedance to the characteristic impedance of the clock trace. The 10pf capacitors are included to help reduce radiated EMI.

Note that the MPC970 also provides the necessary power management controls to allow the operating system to utilize the 601v power management features. Power management is outside the scope of this application note.

Note that clock design issues are non–trivial. System designers should take care to meet the clock skew and other clock timing requirements of the system. For operational details of the MPC970, refer to the MPC970 data sheet. For board wiring guidelines, refer to the *PowerPC 601 System Design Kit* Volume One, Chapter 6.

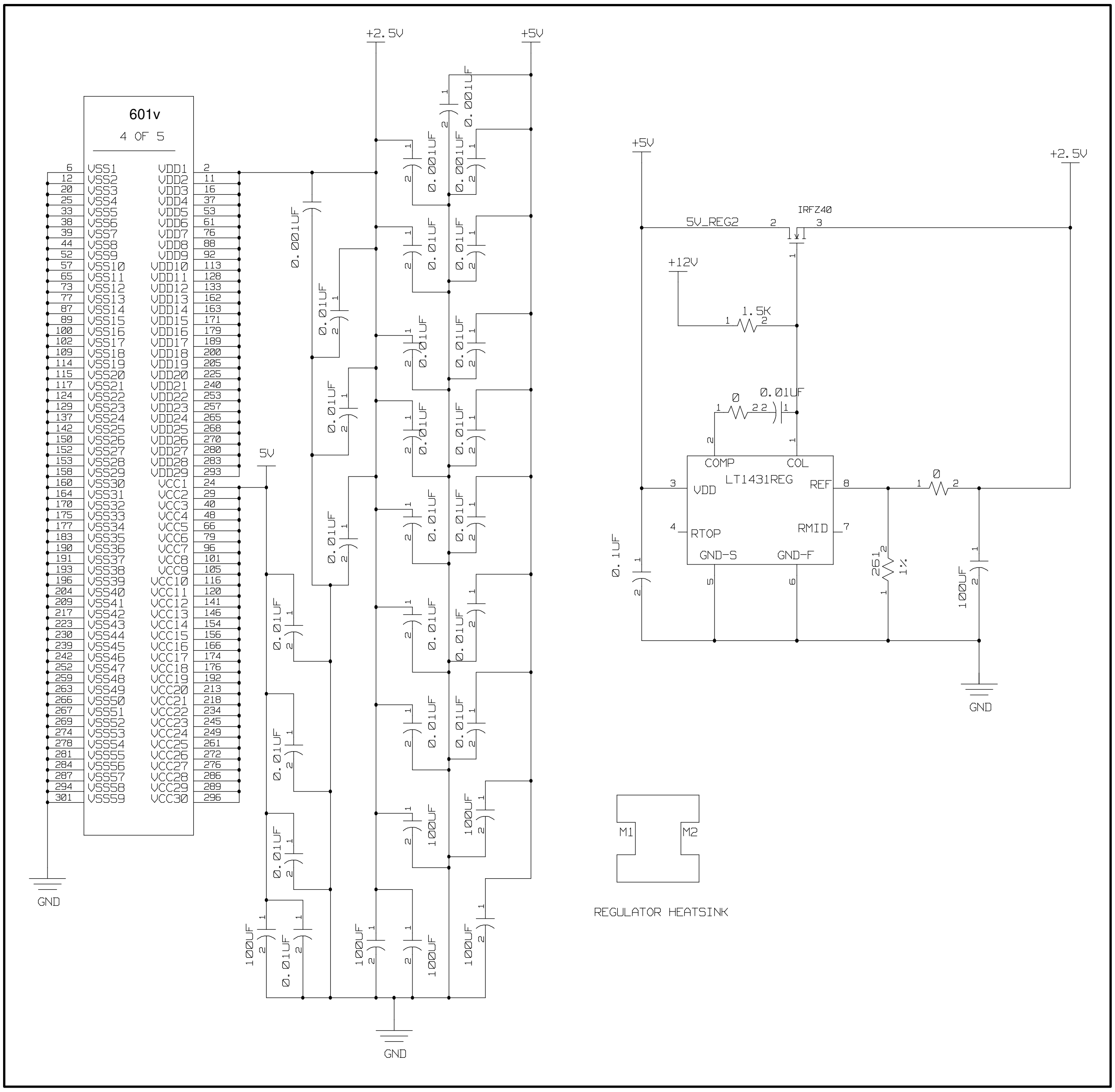

Figure 1

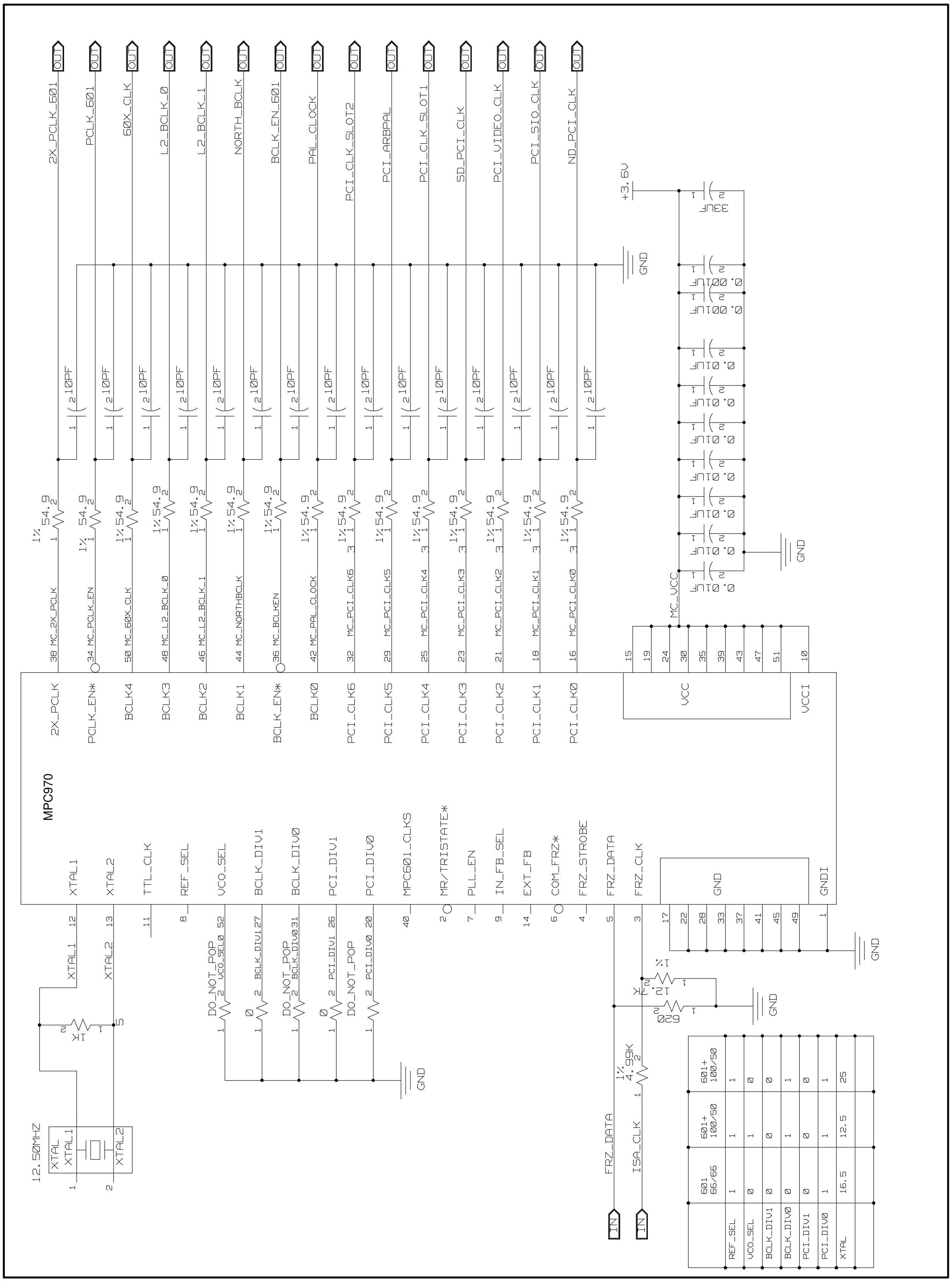
MPC970
2X_PCLK_601
PCLK_601
60X_CLK
L2_BCLK_0
L2_BCLK_1
NORTH_BCLK
BCLK_EN_601
PAL_CLOCK
PCI_CLK_SLOT2
PCI_ARBPAL
PCI_CLK_SLOT1
SD_PCI_CLK
PCI_VIDEO_CLK
PCI_SIO_CLK
ND_PCI_CLK
+3.6V
GND
12.50MHZ
FRZ_DATA
ISA_CLK
REF_SEL 1 1 1
VCO_SEL 0 1 1
BCLK_DIV1 0 0 0
BCLK_DIV0 0 1 1
PCI_DIV1 0 0 0
PCI_DIV0 1 1 1
XTAL 16.5 12.5 25
601 66/66
601+ 100/50
601+ 100/50

Figure 2

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Document Number: MPRA03APU–01